MIL-M-38510/314C
14 July 2003
SUPERSEDING
MIL-M-38510/314B
23 May 1978

## MILITARY SPECIFICATION <br> MICROCIRCUITS, DIGITAL, LOW-POWER SCHOTTKY, TTL, MONOSTABLE MULTIVIBRATORS, MONOLITHIC SILICON

Inactive for new design after 18 April 1997.
This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE
1.1 Scope. This specification covers the detail requirements for monolithic silicon, low-power Schottky TTL, monostable multivibrator microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).
1.2 Part number. The part number should be in accordance with MIL-PRF-38535, and as specified herein.
1.2.1 Device types. The device types should be as follows:

Device type
01
02
03

Circuit
Dual monostable multivibrator, retriggerable, with clear Dual monostable multivibrator, Schmitt trigger inputs, with clear Single monostable multivibrator, retriggerable, with clear
1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.
1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

Outline letter
A GDFP5-F14 or CDFP6-F14
B GDFP4-14
C GDIP1-T14 or CDIP2-T14
D GDFP1-F14 or CDFP2-F14
E GDIP1-T16 or CDIP2-T16
F GDFP2-F16 or CDFP3-F16
2 CQCC1-N20

Terminals

14
14
14
16
16
20

Package style
Flat pack
Flat pack
Dual-in-line
Flat pack
Dual-in-line
Flat pack
Square leadless chip carrier

> Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43216-5000, by using the self addressed Standardization Document improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

### 1.3 Absolute maximum ratings.

| Supply voltage range | -0.5 V dc to 7.0 V dc |
| :---: | :---: |
| Input voltage range | -1.5 V dc at -18 mA to 5.5 V dc |
| Storage temperature range | $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$ |
| Maximum power dissipation per flip-flop, (PD) 1/ |  |
| Device type 01 | 110 mW dc |
| Device type 02 | 149 mW dc |
| Device type 03 | 61 mW dc |
| Lead temperature (soldering, 10 seconds) | $300^{\circ} \mathrm{C}$ |
| Thermal resistance, junction to case ( $\theta_{\mathrm{Jc}}$ ): |  |
| Cases A, B, C, D, E, F, and 2 | (See MIL-STD-1835) |
| Junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) $2 /$. | $175{ }^{\circ} \mathrm{C}$ |

1.4 Recommended operating conditions.

| Supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) | 4.5 V dc minimum to 5.5 V dc maximum |
| :---: | :---: |
| Minimum high level input voltage ( $\mathrm{V}_{\mathrm{IH}}$ ) | 2.0 V dc |
| Maximum low level input voltage ( $\mathrm{V}_{\mathrm{IL}}$ ) | 0.7 V dc |
| Case operating temperature range ( $\mathrm{T}_{\mathrm{C}}$ ) | $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| Minimum pulse width | 40 ns |
| Input pulse rise/fall time, device type 02 |  |
| Schmitt, B input | $1 \mathrm{~V} / \mathrm{s}$ minimum |
| Logic, A input | $1 \mathrm{~V} / \mu \mathrm{s}$ minimum |
| Clear-inactive-state setup time |  |
| Device type 02 | 15 ns minimum |
| External timing resistance, Rext |  |
| Device type 01, 03 | $5 \mathrm{k} \Omega$ minimum, $180 \mathrm{k} \Omega$ maximum |
| Device type 02 | $1.4 \mathrm{k} \Omega$ minimum, $70 \mathrm{k} \Omega$ maximum |
| External timing capacitance, Cext |  |
| Device type 01, 03 | No restriction |
| Device type 02 | 1,000 $\mu \mathrm{F}$ maximum |
| Output duty cycle, device type 02 |  |
| $\mathrm{R}_{\mathrm{T}}=2 \mathrm{k} \Omega$ | 50\% duty cycle maximum |
| $\mathrm{T}_{\mathrm{T}}=70 \mathrm{k} \Omega$ | 90 \% duty cycle maximum |
| Wiring capacitance, Rext/Cext terminal |  |
| Device type 01, 03 (referenced to GND) | 50 pF maximum |

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## 2. APPLICABLE DOCUMENTS

### 2.1 Government documents.

2.1.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Departments of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

## SPECIFICATION

## DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

## STANDARDS

DEPARTMENT OF DEFENSE
$\begin{array}{lll}\text { MIL-STD-883 } & \text { - } \quad \text { Test Method Standard for Microelectronics. } \\ \text { MIL-STD-1835 } & \text { - } & \text { Interface Standard Electronic Component Case Outlines }\end{array}$
(Unless otherwise indicated, copies of the above specifications and standards are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)
2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).
3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
3.3.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figure 1 .
3.3.2 Truth table and functional description. The truth table and functional description shall be as specified on figure 2.
3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.
3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

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3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.
3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.
3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).

## 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
4.2 Screening. Screening shall be in accordance with, MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.
4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).
4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
a. Tests shall be as specified in table II herein.
b. Subgroups 4,5 , and 6 shall be omitted.

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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$ <br> unless otherwise specified | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| High level output voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=-400 \mu \mathrm{~A} \end{aligned}$ | All | 2.5 |  | V |
| Low level output voltage | $\mathrm{V}_{\text {OL }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA} \end{aligned}$ | All |  | 0.4 | V |
| Input clamp voltage | VIC | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=-18 \mathrm{~mA}, \\ & \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \end{aligned}$ | All |  | -1.5 | V |
| Low level input current | ILL1 | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0.4 \mathrm{~V}$ | 01, 03 | -160 | -400 | $\mu \mathrm{A}$ |
| Low level input current at clear input | $\mathrm{I}_{\text {IL2 }}$ |  | 02 | -30 | -680 |  |
| Low level input current at $\mathrm{A}_{\text {IN }}$ |  |  | 02 | -30 | -400 |  |
| Low level input current $\mathrm{B}_{\text {IN }}$ |  |  | 02 | -30 | -580 |  |
| High level input current | $\mathrm{I}_{\mathrm{H} 1}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=2.7 \mathrm{~V}$ | All |  | 20 | $\mu \mathrm{A}$ |
| High level input current | $\mathrm{I}_{1 \mathrm{H} 2}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ | All |  | 100 |  |
| Short circuit output current | los | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{H}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{GND} \end{aligned}$ | All | -15 | -130 | mA |
| Supply current (quiescent) | $\mathrm{ICC1}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | 02 |  | 11 | mA |
| Supply current (quiescent or triggered) | $\mathrm{ICC2}$ |  | 01 |  | 20 |  |
| Supply current (triggered) | Icca |  | 02 |  | 27 |  |
| Propagation delay time low to high level from input A | $\mathrm{tPLH1}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 5 \%, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \mathrm{Cext}=\underline{1} / \\ & \text { Rext }=\underline{1} / \end{aligned}$ | 01, 03 | 5 | 57 | ns |
|  |  |  | 02 | 5 | 113 |  |
| Propagation delay time low to high level from input B | tPLH2 |  | 01, 03 | 5 | 74 |  |
|  |  |  | 02 | 5 | 90 |  |
| Propagation delay time low to high level from clear | tplH3 |  | 01, 03 | 5 | 75 |  |
|  |  |  | 02 | 5 | 105 |  |
| Propagation delay time high to low level from input A | $\mathrm{t}_{\text {PHL1 }}$ |  | 01, 03 | 5 | 75 |  |
|  |  |  | 02 | 5 | 128 |  |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$ <br> unless otherwise specified | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Propagation delay time high to low level from input B | $\mathrm{t}_{\text {PHL2 }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 10 \% \\ & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \mathrm{Cext}=\underline{1} / \\ & \text { Rext }=\underline{1 /} \end{aligned}$ | 01, 03 | 5 | 92 | ns |
|  |  |  | 02 | 5 | 105 |  |
| Propagation delay time high to low level from clear | $\mathrm{t}_{\text {PHL3 }}$ |  | 01, 03 | 5 | 48 | ns |
|  |  |  | 02 | 5 | 90 |  |
| Minimum pulse width of Q output | $\mathrm{tP}_{\text {(MIN }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 10 \% \\ & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \mathrm{Cext}^{2}=\underline{2} / \pm 10 \% \\ & \text { Rext }=\underline{2} / \pm 10 \% \end{aligned}$ | 01, 03 |  | 308 | ns |
| Width of Q output pulse | $\mathrm{t}_{\text {1 }}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \text { Cext }=\underline{2} / \pm 10 \% \\ & \mathrm{Rext}=\underline{2} / \pm 10 \% \end{aligned}$ | 02 | 20 | 91 |  |
|  | tp2 |  | 02 | 70 | 195 |  |
|  | $\mathrm{t}_{\text {P }}$ |  | 02 | 600 | 850 |  |
|  | tp4 |  | 01, 03 | 3.0 | 6.25 | $\mu \mathrm{s}$ |
|  | tp5 |  | 02 | 5.5 | 8.5 | ms |

1/ For propagation delay tests, see table III for Cext and Rext values.
2/ $\mathrm{tp}_{\text {(MIN) }}$ test, Cext $=$ open and Rext $=5 \mathrm{k} \Omega$.
$t_{p 1}$ test, Cext $=$ open and Rext $=2 \mathrm{k} \Omega$.
tp2 test, Cext $=80 \mathrm{pF}$ and Rext $=2 \mathrm{k} \Omega$.
tp3 test, Cext $=100 \mathrm{pF}$ and Rext $=10 \mathrm{k} \Omega$.
$t_{p 4}$ test, Cext $=1,000 \mathrm{pF}$ and Rext $=10 \mathrm{k} \Omega$.
tps test, Cext $=1 \mu \mathrm{~F}$ and Rext $=10 \mathrm{k} \Omega$.

TABLE II. Electrical test requirements.

| MIL-PRF-38535 <br> test requirements | Subgroups (see table III) |  |
| :--- | :--- | :--- |
|  | Class S <br> devices | Class B <br> devices |
| Interim electrical parameters | 1 | 1 |
| Final electrical test parameters | $1^{*}, 2,3,7,9$, <br> 10,11 | $1^{*}, 2,3,7,9$ |
| Group A test requirements | $1,2,3,7,8$, | $1,2,3,7,8$, |
|  | $9,10,11$ | 9 |
| Group B electrical test parameters | $1,2,3$ | $\mathrm{~N} / \mathrm{A}$ |
| when using method 5005 QCI option | $9,10,11$ |  |
| Group C end-point electrical parameters | $1,2,3$, | $1,2,3$ |
|  | $9,10,11$ |  |
| Additional electrical subgroups for | $\mathrm{N} / \mathrm{A}$ | 10,11 |
| group C inspections | $1,2,3$ | $1,2,3$ |
| Group D end-point electrical parameters |  |  |

*PDA applies to subgroup 1.
4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.
4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
a. End-point electrical parameters shall be as specified in table II herein.
b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
c. Subgroups 3 and 4 shall be added to group $C$ inspection parameters for class $B$ devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.
4.5 Methods of inspection. Methods of inspection shall be specified and as follows:
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

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$$
\frac{\text { DEVICE TYPE } 01}{\text { CASES E AND F }}
$$



CASE 2


FIGURE 1. Terminal connections.

$$
\frac{\text { DEVICE TYPE } 02}{\text { CASES E AND F }}
$$



FIGURE 1. Terminal connections - Continued.


FIGURE 1. Terminal connections - Continued.

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Device type 01 and 02

| INPUTS |  |  | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: |
| CLEAR | A | B | Q | $\overline{\mathrm{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | $\uparrow$ | $\sqcap$ | $\sqcup$ |
| H | $\downarrow$ | H | $\sqcap$ | $\sqcup$ |
| $\uparrow$ | L | H | $\sqcap$ | $\sqcup$ |

Device type 03

| INPUTS |  |  |  |  | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLEAR | A1 | A2 | B1 | B2 | Q | $\overline{\mathrm{Q}}$ |
| L | X | X | X | X | L | H |
| X | H | H | X | X | L | H |
| X | X | X | L | X | L | H |
| X | X | X | X | L | L | H |
| H | L | X | $\uparrow$ | H | $\sqcap$ | $\sqcup$ |
| H | L | X | H | $\uparrow$ | $\sqcap$ | $\sqcup$ |
| H | X | L | $\uparrow$ | H | $\sqcap$ | $\square$ |
| H | X | L | H | $\uparrow$ | $\sqcap$ | $\sqcup$ |
| H | H | $\downarrow$ | H | H | $\sqcap$ | $\sqcup$ |
| H | $\downarrow$ | $\downarrow$ | H | H | $\sqcap$ | $\sqcup$ |
| H | $\downarrow$ | H | H | H | $\sqcap$ | $\sqcup$ |
| $\uparrow$ | L | X | H | H | $\sqcap$ | $\square$ |
| $\uparrow$ | X | L | H | H | $\sqcap$ | $\square$ |

NOTES:

1. $H=$ high level (steady state), $L=$ low level (steady state), $\uparrow=$ transition from low to high level,
$\downarrow=$ transition from high to low level, $\square=$ one high level pulse, $\square=$ one low level pulse, $\mathrm{X}=$ irrelevant (any input, including transitions).
2. To use the internal timing resistor of device type 03 connect Rint to $\mathrm{V}_{\mathrm{cc}}$.
3. An external timing capacitor may be connected between Cext and Rext/Cext (positive).
4. For accurate repeatable pulse widths, connect an external resistor between Rext/Cext and $V_{c c}$ with Rint open circuited.
5. To obtain variable pulse widths, connect external variable resistance between Rint or Rext/Cext and $\mathrm{V}_{\mathrm{cc}}$.

FIGURE 2. Truth table and functional description.

## Device types 01 and 03

This multivibrator features d-c triggering from gated low level active (A inputs), and high level active (B inputs). Output pulse width is a function of external capacitor and resistor values. Retriggering of input before output terminates, extends output pulse width. Overriding clear feature permits termination of output pulse width at a predetermined time independent of R and C timing components.


B INPUT


## NOTE:

Retrigger pulse must not start before
0.22 Cext (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 2. Truth table and functional description - Continued.

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## Device type 01 and 03 (Continued)

The output pulse width ( tp ) is a function of the external capacitor and resistor values.
For output pulse widths when Cext $>1,000 \mathrm{pF}, \mathrm{tp}$ is defined as :
$t p \approx 0.4 R_{T}$ Cext Where $R_{T}$ is in $k \Omega$, Cext is in $p F$, and $t p$ is in ns.
For output pulse widths when Cext $<1,000 \mathrm{pF}$, tp is defined as:


NOTE:
This value of resistance exceeds the maximum recommended for use over the full temperature range

FIGURE 2. Truth table and functional description - Continued.

## Device type 02

This multivibrator features a negative transition triggered input and a positive transition triggered input, either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level, not directly related to transition time of input pulse. Once fired, the outputs are independent of further transitions of $A$ and $B$ inputs, and are a function of the timing components. Output pulses can be terminated by the overriding clear, independent of $R$ and $C$ timing components.


FIGURE 2. Truth table and functional description - Continued.

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## Device type 02 (Continued)

The output pulse width (tp) is a function of the external capacitor and resistor values.
The output pulse width is defined as :
$t p \approx 0.7 R_{T}$ Cext Where $R_{T}$ is in $k \Omega$, Cext is in $p F$, and tp is in ns.


FIGURE 2. Truth table and functional description - Continued.


TIMING COMPONENT CONNECTIONS

FIGURE 2. Truth table and functional description - Continued.


FIGURE 3. Switching test circuit and waveforms for device types 01 and 03.


## NOTES:

1. Pulse generator has the following characteristics: PRR $\leq 1.0 \mathrm{MHz}, \mathrm{t}_{\mathrm{PIN}} \geq 40 \mathrm{~ns}, \mathrm{t}_{\mathrm{THL}} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{TLH}} \leq 15 \mathrm{~ns}$, and $Z_{\text {out }}=50 \Omega$.
2. See table III notes for Rext, Cext values.
3. $C_{L}=50 \mathrm{pF} \pm 10 \%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. All diodes are 1 N3064, or 1 N916 or equivalent.
5. Load circuit on a given output is only required where the specified test in table III indicates "OUT" on that output.
6. $\mathrm{t}_{\text {SETUP }}$ (max) shall be $\leq 50 \%$ of the typical output pulse width for the actual Cext used (see figure 2).

FIGURE 3. Switching test circuit and waveforms for device types 01 and 03 - Continued.


FIGURE 4. Switching test circuit and waveforms for device type 02.


## NOTES:

1. Pulse generator has the following characteristics: $\mathrm{PRR} \leq 1.0 \mathrm{MHz}, \mathrm{t}_{\mathrm{PIN}} \geq 40 \mathrm{~ns}, \mathrm{t}_{\mathrm{T}_{\mathrm{HL}}} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{TLH}} \leq 15 \mathrm{~ns}$, tsetup 1 (CLEAR INACTIVE) $=15 \mathrm{~ns}$ and Zout $=50 \Omega$.
2. See table III notes for Rext, Cext values.
3. $C_{L}=50 \mathrm{pF} \pm 10 \%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. All diodes are 1 N3064, or 1 N916 or equivalent.
5. Load circuit on a given output is only required where the specified test in table III indicates "OUT" on that output.
6. $\mathrm{t}_{\text {SETUP }}$ (max) shall be $\leq 50 \%$ of the typical output pulse width for the actual Cext used (see figure 2).

FIGURE 4. Switching test circuit and waveforms for device type 02-Continued.
TABLE III. Group A inspection for device type 01.

See footnotes at end of this table.
TABLE III. Group A inspection for device type 01.

> A. $\mathrm{V}_{\mathbb{I}}=3.0 \mathrm{~V}$ minimum.
B. $\mathrm{V}_{\mathbb{I}}=0.0 \mathrm{~V}$ or GND .
C. Apply input pulse
D. Test numbers 39 through 55 shall be run in sequence.
E. Output voltages shall be either:

$$
\mathrm{H}>1.5 \mathrm{~V} \text {; } \mathrm{L}<1.5 \mathrm{~V}
$$

F. Rext $=5 \mathrm{k} \Omega$ minimum to $180 \mathrm{k} \Omega$ maximum, connected to $\mathrm{V}_{\mathrm{Cc}}$; Cext $\leq 1,000 \mu \mathrm{~F}$, connected to Rext terminal.
> G. Rext $=5 \mathrm{k} \Omega \pm 10 \%$, connected to $\mathrm{V}_{\mathrm{cc}}$.
> I. Rext $=10 \mathrm{k} \Omega \pm 10 \%$, connect to $\mathrm{V}_{\mathrm{cc}}$; Cext $\leq 1,000 \mu \mathrm{~F} \pm 10 \%$, connected to Rext terminal.
> J. During subgroups 9, 10, 11 testing, Rext and Cext may remain applied on the side of the
> J. During subgroups $9,10,11$ testing, Rext and Cext may remain applied on the side of the device not under test if desired
K. For circuit D, I I IL1 limits are 120 mA to 360 mA .
> L. Rext $=10 \mathrm{k} \Omega \pm 10 \%$, connect to $\mathrm{V}_{\mathrm{cc}}$; Cext $\geq 45 \mathrm{pF}$ connected to Rext terminal.
NOTES:
TABLE III. Group A inspection for device type 02

See footnotes at end of this table.
TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high $\geq 2.0 \mathrm{~V}$, low $\leq 0.7 \mathrm{~V}$,



F. Rext $=1.4 \mathrm{k} \Omega$ minimum to $70 \mathrm{k} \Omega$ maximum, connected to $\mathrm{V}_{\mathrm{cc}} ; \mathrm{Cext} \leq 1,000 \mu \mathrm{~F}$, connected to Rext terminal.
G. Rext $=2 \mathrm{k} \Omega \pm 10 \%$, connected to $\mathrm{V}_{\mathrm{cc}}$ Cext $=80 \mathrm{pF} \pm 10 \%$, connected to Rext terminal.
I. Rext $=10 \mathrm{k} \Omega \pm 10 \%$, connect to $\mathrm{V}_{\mathrm{cc}}$; Cext $=100 \mathrm{pF} \pm 10 \%$, connected to Rext terminal.
J. Rext $=10 \mathrm{k} \Omega \pm 10 \%$, connect to $\mathrm{V}_{\mathrm{cc}}$; Cext $=1.0 \mu \mathrm{~F} \pm 10 \%$, connected to Rext terminal.

$$
\text { K. Rext }=2 \mathrm{k} \Omega \pm 10 \% \text {, connect to } \mathrm{V}_{\mathrm{cc}} \text {. }
$$

L. Note F may apply during subgroups 1,2 , and 3 testing if desired.
M. During subgroups $9,10,11$ testing, Rext and Cext may remain applied on the side of the device not under test if desired.
N. Rext $=10 \mathrm{k} \Omega \pm 10 \%$, connect to $\mathrm{V}_{\mathrm{cc}} ;$ Cext $\geq 45 \mathrm{pF}$ connected to Rext terminal.
TABLE III. Group A inspection for device type 03.

TABLE III. Group A inspection for device type 03 - Continued.


[^1]
## 5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.
6. NOTES
(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)
6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
6.2 Acquisition requirements. Acquisition documents should specify the following:
a. Title, number, and date of the specification.
b. Complete part number (see 1.2).
c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirements for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
j. Requirements for "JAN" marking.
6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.
6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

| GND | Ground zero voltage potential |
| :---: | :---: |
| 1 l | Current flowing into an input terminal |
| $V_{\text {IC }}$ | Input clamp voltage |
| V IN | Voltage level at an input terminal |

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
6.7 Substitutability. The cross-reference information below is presented for the convenience of users.

Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

| Military device <br> type | Generic-industry <br> type |
| :---: | :---: |
| 01 | $54 \mathrm{LS} 123,74 \mathrm{LS} 123$ |
| 02 | $54 \mathrm{LS} 21,74 \mathrm{LS} 21$ |
| 03 | $54 \mathrm{LS} 122,74 \mathrm{LS} 122$ |

6.8 Manufacturers' designation. Manufacturers' circuits, which form a part of this specification, are designated as shown in table IV herein.

TABLE IV. Manufacturers' designation.

| Manufacturers |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Device <br> type | A | B | C | D | E |  |
|  | Texas Instru- <br> ments Inc. | Signetics <br> Corporation | National <br> Semiconductor <br> Corp | Motorola <br> Inc | Raytheon <br> Company |  |
|  | X |  | X | X |  |  |
| 02 | X | X | X | X |  |  |
| 03 | X |  | X | X | X |  |

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

| Custodians: | Preparing activity: |
| :--- | :---: |
| Army - CR | DLA - CC |
| Navy - EC | (Project 5962-1964) |
| Air Force -11 |  |
| DLA - CC |  |

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

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1. DOCUMENT NUMBER <br>
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2. DOCUMENT DATE (YYYYMMDD) <br>
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3. DOCUMENT TITLE

MICROCIRCUITS, DIGITAL, LOW-POWER SCHOTTKY TTL, MONOSTABLE MULTIVIBRATORS, MONOLITHIC SILICON
4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)
5. REASON FOR RECOMMENDATION

| 6. SUBMITTER |  |  |
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| a. NAME (Last, First Middle Initial) | b. ORGANIZATION |  |
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| 8. PREPARING ACTIVITY |  |  |
| a. NAME <br> Defense Supply Center, Columbus | b. TELEPHONE (Include Area Code <br> (1) Commercial 614-692-0536 | (2) DSN 850-0536 |
| c. ADDRESS (Include Zip Code) DSCC-VA <br> P. O. Box 3990 <br> Columbus, Ohio 43216-5000 | IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: <br> Defense Standardization Program Office (DLSC-LM) <br> 8725 John J. Kingman Road, Suite 2533 <br> Fort Belvoir, Virginia 22060-6221 <br> Telephone (703)767-6888 DSN 427-6888 |  |


[^0]:    1/ Must withstand the added $P_{D}$ due to short-circuit test (e.g., los).
    2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.

[^1]:    NOTES:
    C. For circuit D, IIL1 limits are 120 to 360 mA .
    D. Test numbers 29 through 45 shall be run in sequence.
    E. Output voltages shall be either:
    F. Cext connected to Rext/Cext through a $1,000 \mathrm{pF} \pm 10 \%$ capacitor.
    G. Rext/Cext connected to $\mathrm{V}_{\mathrm{cc}}$ through a $5 \mathrm{k} \Omega \pm 10 \%$ resistor.
    Note K may apply during subgroups 1 , 2 , and 3 testing if desired.
    $--2.5 \mathrm{~V} \min / 5.5 \mathrm{~V}$ max.
    $-\quad 0 \mathrm{~V}$
    K. Rext/Cext connected to $\mathrm{V}_{\mathrm{Cc}}$ through a $5 \mathrm{k} \Omega$ to $180 \mathrm{k} \Omega$ resistor, and Cext connected to Rext/Cext through a $\leq 1,000 \mu \mathrm{~F}$ capacitor.
    M. Cext connected to Rext/Cext through $\mathrm{A} \geq 45 \mathrm{pF}$ capacitor, Rext/Cext connected to $\mathrm{V}_{\text {cc }}$ through a $10 \mathrm{k} \Omega \pm 10 \%$ resistor. N. Rext/Cext connected to $\mathrm{V}_{\mathrm{cc}}$ through a $10 \mathrm{k} \Omega \pm 10 \%$ resistor.

